ABSTRACT

CONTEXT PRESERVATION

A processor which is switchable between a first execution mode (such as a scalar mode) and a second execution mode (such as a VLIW mode) is disclosed. The processor has a first processor context when in the first execution mode and a second processor context, different from the first processor context, when in the second execution mode. The processor generates an exception when the processor attempts to change from one execution mode to the other. When the processor switches to a thread of execution which is in the first execution mode, or when the processor switches to a thread of execution which was the last thread to be in the second execution mode, only the first processor context is preserved. The processor may be arranged such that the number of threads that may be in the second execution mode at any one time is less than the total number of threads that may be active on the processor at any one time.

(Figure 5)